Imaging with
CCDs and CMOS Imagers

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**Imaging Systems - detectors**

1024x1024 HgCdTe IR array

CMOS imager

2048x2048 CCD

90Prime focal plane

Magacam focal plane for MMT
**CCD Architectures**

*Full frame*
- entire area of CCD used to collect image
- best use of area, most common in astronomy
- requires a shutter during readout

*Frame transfer*
- *frame store* half of CCD covered with opaque mask
- *image store* half is unmasked and collects photons during integration
- rapid shift (1 – 100 millisecond) from image store to frame store after exposure (image and store parallel clocks must be separate)
- frame store read slowly while image store integrates next exposure
- reduces “dead time”
- no shutter required
- only half of silicon area collects light
CCD Architectures

Interline transfer

– opaque transfer bus along each column
– rapid shift from each pixel (or photodiode) to bus after exposure
– bus pixels readout during next exposure
– reduces dead time
– no shutter required
– significant opaque area
– fill factor < 1 even in image area

Possible to increase fill factor by using *microlenses*, typically made by applying photoresist to surface, etching, and thermal processing to produce lens shape.
CCD Architectures—SITe CCD
Charge Transfer

- Charge in a pixel after N pixel shifts is \( S_N = S_i (CTE)^N \) where \( S_i \) is initial charge in pixel before shifting.

- The charge found \( n \) pixels after target pixel \( (S_i) \) following N pixel shifts is \( S_{N+n} = \frac{S_i (N \cdot CTI)^n}{n!} \exp(-N \cdot CTI) \).

Example: An Fe-55 X-ray event (1620 e\(^-\)) in the far corner of a 4k\times4k device will contain only 1493 e\(^-\) at the output amplifier if CTE = 0.999990 (92%)!
**Problems - CTE**

- line trap – typically due to a short between phases in the image area
- parallel clock voltage at gates near short are reduced
- increased applied gate voltage increase normally reduces trap size by increasing effective $V_{\text{gate}}$ near trap
- *fat zero* or *preflash* may fill traps – very low level exposure or direct input before integration exposure

*global CTE problem – silicon problem?*
2- and 4-phase CCD Clocking

implant modifies channel potential
Pixel Binning

- Timing pattern may be changed so charge from multiple pixels are added together.
- Decreases spatial resolution of detector as bigger effective pixels.
- Allows high charge capacity (larger dynamic range).
- Increases read out speed since each pixel is not sampled at output.
- Binning can be performed in columns or rows, with not necessarily the same binning factor.
- Serial register pixels are usually made 2x the size of image pixels to allow 2x charge capacity.
- Many CCDs have an Output Summing Well which is the last pixel of a serial register, independently clocked, and 2x the size of a serial pixel, to aid in binning.
- Also called noiseless co-addition since summing comes before readout, when read noise is generated.
- For a shot-noise limited, uniform exposure,

\[ SNR = \left[ P_H P_s S(e^-) \right]^{1/2} \]

where \( S(e^-) \) is the average unbinned signal in electrons per pixel
Dark Current

\[ D(e^-) = 2.5 \times 10^{15} A_{\text{pix}} D_{\text{FM}} T^{1.5} e^{-E_g / 2kT} \]

DFM is nA/cm\(^2\) @300K

A\(_{\text{pix}}\) pixel area (cm\(^2\))

parameter is pA/cm\(^2\) @ 293K
**Back Illuminated CCDs**

- Optical absorption and multiple reflections from frontside structures (polysilicon gates and oxides) reduce efficiency
- No blue/UV transmission through polysilicon
- Solution is the thin CCD and illuminate device from backside.
- Must remove highly doped p+ material which CCD is fabricated with to leave only epitaxial material. Typically 10-20 microns thick.
- Interference fringing is worse than for thick devices.
- If a field free region remains, between back surface and edge of depletion region, then charge spreading occurs and resolution is degraded. Worse in the blue.
- Backside surface is a disrupted silicon crystal which has dangling bonds, creating a positively charged interface. This traps electrons at the backside.
- A freshly thinned CCD has very poor QE.
- Adding a negative charge to the back surface is called *backside charging* and lead to very high QE devices (with AR coatings).
ITL Backside CCD Processing Flow

The following process steps are performed after device fabrication, which leads to high cost of back illuminated CCDs:

- Select via wafer probing
- Mechanically lap
- Dice
- Hybridize
- Wax protection of edges
- Selective etch
- Epitaxial etch
- Oxidize
- Chemisorption charge
- Antireflection coat
- Package
- Characterize
UA Foundry Wafer

- STA design and fabrication through DALSA
- ITL post-fabrication processing
- 2 4kx4k CCDs
- 4 2688x512 CCDs
- 4 1200x800 CCDs
- 512x1024 FT guiders
- 128x128 AO devices
- FBI test devices

There are very few fabs in the world making scientific CCDs.
STA0500A Back Illuminated CCD

STA0500 4kx4k
15 \( \mu \text{m} \) pixels

- typical hybridized large format CCD
- CCD hybridized to thick silicon substrate
- indium and gold bumps
- epoxy underfill
- die attached & wire bonded to Kovar package
Cold Probe Station

Modified Electroglas 2001X Probe System
Hybridization

- Flip chip bonders used to align and bond detector and substrate
- Infrared aligner for silicon substrates
- Split field aligner for non-IR transparent materials
Acid Etching

• 1:3:8 HF:HNO₃:CH₃COOH acid solution used to etch p⁺ substrate to epitaxial interface
• Etch selectivity critical to achieve uniform thickness
• Typical doping levels
  \[ p^+ = 10^{18} \text{ cm}^{-3}, \quad p = 10^{15} \text{ cm}^{-3} \ (10 - 250 \ \Omega\text{-cm}) \]
Backside Potential Well

$p^+$ material removed

SiO₂

$p$-Si

frontside gate

n-buried channel

-native positive charge

-desired negative charge

$hν$
**Field Free Region – Charge Spreading**

The region in a back illuminated CCD between the edge of the depletion region and the back surface is the “field-free” region. Photogenerated electrons can diffuse in all directions in this region, reducing resolution through charge spreading.

Experimentally,

\[
C_{ff} = 2x_{ff} \left(1 - \frac{L}{x_{ff}}\right)^{1/2}
\]

\(C_{ff}\) is the lateral diffusion diameter, \(x_{ff}\) is the field free thickness, and \(L\) is the distance from the backside surface where the photoelectron is generated.

5 \(\mu\)m FF region => 10 \(\mu\)m electron cloud

higher resistivity material has deeper depletion region, so \(x_{ff}\) is smaller. 50 \(\Omega\) cm material typical, but 1000-10,000 \(\Omega\) cm possible.

Note depletion depth is proportional to \(1/\sqrt{N_A}\).
Charge Diffusion – X-ray image

these are single pixel events from an Fe-55 X-ray source with 2 CCDs ~ 17 µm thick

30 Ω cm Si

150 Ω cm Si
Pt catalyzes both oxygen and hydrogen...

\[
\begin{align*}
H_2 + Pt_{\text{cat}} & \rightarrow 2H_{\text{adsorbed}} \\
O_2 + Pt_{\text{cat}} & \rightarrow 2O_{\text{adsorbed}} \\
H_{\text{ads}} & \rightarrow H^+ + e^- \\
O_{\text{ads}} + e^- & \rightarrow O^-
\end{align*}
\]

\(O^-\) charges CCD back surface
\(H^+\) discharges surface
Backside charging with Pt causes *temperature dependent QE variations* because back surface is not pinned with the negative charge density required to drive all photoelectrons to frontside.
UA Chemisorption Process Steps – Backside Charging

- Oxidize backside of thinned CCD to reduce interface trap density
- Apply thin metal film (10A silver) to promote negative backside charge
- Apply antireflection coating optimized for spectral region of interest
Backside CCD QE

![Graph showing measured QE for different CCDS across various wavelengths.](image-url)
Backside CCD QE - Ultraviolet
Packaging - Profilometer

- Interchangeable optical pens using white light chromatic aberration technique
- 300 mm XY travel
- Referenced to optical flat
- Non-contact
- 10 nm min. accuracy
- 24 mm max range
TDI – Time Delay and Integrate or Drift Scanning

• If a CCD is aligned with columns east-west on the sky, charge can be clocked out at sidereal rate to form an image with an open shutter and no telescope movement.

• Alternate schemes allow combination of telescope tracking and non-sidereal rate clocking.

• Resultant image is a East-West strip.

• Plate scale S in arcsec/pixel, \( S = 206.265 \times P/F \), where \( P \) pixel size \( \mu m \), \( F \) focal length mm.

• Drift rate \( R \) (sec/pix) \( R = \frac{86164.09[sec/sidereal\ day]}{(360 \times 3600\ arcsec)\cos\delta} S \)

• Each part of image is averaged over many pixels, so \( PRNU \) is minimized.

Problems:

1) stars smears in RA because only one declination is exactly tracked (stars closer to celestial pole drift slower across detector).

2) stars trace an arc across detector, smearing in declination.

TDI also used for airborne imaging, machine vision, etc.

*TDI image from Auckland*
Orthogonal Transfer CCDs - OTCCDs

• Orthogonal transfer devices replace channel stop with a clocked phase, so clocking in both axis directions can be achieved.
• If centroiding is performed with another detector, the feedback can be used to clock the OTCCD in any direction at high speed to minimize image blurring.
• OTCCDs are therefore most useful for high resolution imaging, eliminating the need for mechanical motion compensation such as tip/tilt mirrors.
• Problems include complexity (yield) and charge traps or pockets, which can be enhanced due to repetitive clocking.

A 5 electron trap will hold 5 electrons even as charge is shifted out of the pixel. Repetitive clocking enhanced loss.

MIT/LL and John Tonry @ Univ. Hawaii
The Orthogonal Transfer Array (OTA)

Pan-STARRS project will use OTAs, which monolithic arrays of OTCCDs

Advantages include low susceptibility to internal shorts and restriction of full well blooming to single OTCCD cells. Low shorts->high yield->low cost
OTA for WIYN One Degree Imager
Fully Depleted Devices

- Fully depleted (300 μm thick at LBL, 50 μm thick commercially).
- Greatly reduced interference fringing and very high near-IR QE.
- Backside bias contact required for depletion. Must be transparent.
- Very high resistance (ultra pure) silicon required to support complete depletion.
- Problems include sensitivity to cosmic rays, higher dark current, backside contact, and charge spreading (resolution loss).

300 μm fully depleted CCD QE
Fully Depleted LBNL CCD - SNAP
Cosmic Rays

CCDs are great cosmic ray detectors!

Remove with multiple images

Thicker devices are more sensitive

cosmic rays are high energy (MeV) particles (protons, alphas, electrons, positrons, etc.)

rate very approximately 100 cm$^{-2}$ hr$^{-1}$
**Detectors with Internal Gain**

Some non-photoemissive detectors can also have electron gain and may be used for photon counting or very low light level applications.

- *Avalanche photodiodes* have gain due to impact ionization when the photoelectron is accelerated in a very high electric field within the silicon.
- *L3 technology* from E2V, Inc. utilizes an extending serial register and a very high electric field within a pixel. As the CCD shifts charge through this extended register, a small avalanche gain (1.01) is achieved. After ~100 gain stages, an electron packet larger than the read noise is generated and photon counting is possible.
Quantum Efficiency

The absorptive quantum efficiency $Q_E_{\text{abs}}$ is the fraction of incident photons which is absorbed in the detector,

$$Q_E_{\text{abs}} = (1 - r)\frac{S_0 - S_0 e^{-a(\lambda)x}}{S_0} = (1 - r)(1 - e^{-a(\lambda)x})$$

where $x$ is the thickness of the detector and $r$ is the reflectivity from the incident surface.

Increase QE by…

1. reducing reflectivity with antireflection (AR) coatings
2. increasing absorption coefficient (material selection)
3. increasing thickness of absorbing material
Quantum Efficiency vs. Detector Thickness

uncoated silicon 300K
Interference Fringing in Detectors

When the absorption length is large compared to the detector thickness, light can reflect multiple times between the front and back surfaces of a detector. This leads to constructive and destructive optical interference within the detector.
Silicon Reflectivity – including absorption

- Illuminant: WHITE
- Medium: AIR
- Substrate: SI
- Exit: SI
- Detector: IDKAL
- Angle: 0.0 (deg)
- Reference: 0.55 (μm)
- Polarization: Ave
- First Surface: Front

Reflectance (%) vs Wavelength (μm)
Antireflection Coatings

• An AR coating is a thin film stack applied to the detector surface to decrease reflectivity; typically used on all modern imagers.
• Coating materials should have proper indices and be non-absorbing in the spectral region of interest.
• With absorbing substrates which have indices with strong wavelength dependence (like silicon), thin film modeling programs are required to calculate reflectivity.
• Designer must consider average over incoming beam (f/ ratio) and angle of incidence due to angular dependence.

Anti-reflection coatings work by producing two reflections which interfere destructively with each other.
Silicon Reflectivity – AR Coatings

- Uncoated Si
- 1 layer - 550 A HfO₂
- 2 layer - 500 A HfO₂ + 1000A MgF₂

Reflectance (%) vs Wavelength (μm)
Quantum Yield

One energetic interacting photon may create multiple electrons-hole pairs through collision (impact ionization) of electrons in conduction band.

\[ QY = \frac{E}{E_{e-h}} \]

is the Quantum Yield, \( E_{e-h} \) is energy per electron hole pair

\[ E_{e-h, Si} = 3.65 \frac{eV}{e^-} \] for \( E > 3.1 \text{ eV} \) (~0.4 um)

\[ \lambda (\mu m) = \frac{1.239}{E(eV)} \]

A 5.9 keV x-ray photon (Fe-55) will create ~1620 electrons per photon in Si
CMOS Imagers
CMOS Imager Architecture

CMOS imagers utilize a CMOS fabrication process to create an array of photosensors, typically photodiodes. Common devices are *monolithic* in which readout circuitry is on the same device as the photosensors or *hybrid* in which the detector is hybridized or flip chip bonded to the readout.

Called *active pixel sensors* (APS) or *passive pixel sensors* (PPS), depending on pixel structure.
CMOS Imager Architecture

1025x1024 photodetector array

32 reset/select skip blocks, resp., row scan

exposure control

4-channel readout

CDS, S&H

8 column scan skip blocks,
4-channel column control
**CMOS Advantages**

- Very low power usage – no high voltage required for depletion, no large clock voltage swings for charge transfer, little off-chip electronics, 5 or 3.3 V operation.
- Radiation tolerate – CMOS fabrication process.
- ULSI – digital circuitry allows “on-chip” processing functions, such as ADC, logarithmic gain, multiple sampling, image compression, anti-jitter, color, etc.
- Random access of pixels – charge to voltage conversion at each pixel.
- No CTE issues as no charge transfer – less susceptible to traps.
- CMOS compatible with 90% of silicon fabrication facilities.

Single power source in and digital output is very attractive!
4kx4k 15 um pixel CMOS Imager

Micron Technology, Inc.- largest CMOS imager
CMOS Disadvantages

• *Fill factor* is relative size of photosensor to pixel size. Smaller scale *design rules* for fabrication allow higher fill factor, but is always < 100%. Typically <50%.

• Noise higher than CCD due to amplifier designs which must drive busses with higher current.

• Fixed pattern noise high compared to CCDs due to pixel to pixel and column to column gain variations (thousands of amplifiers and capacitors!). Typically 0.1 – 3% variations. Very complex integrated circuits.

• Circuitry generates heat which increases (local) dark current.

• Shallow p-n junctions of CMOS processes limit light sensitivity.
One technique to improve fill factor is to use implants to create internal electric fields to channel photogenerated electrons to photodiode.
Back Illuminated CMOS Imagers

- Same issues as for CCDs
- Illuminate from backside to enhance QE
- Avoid stimulating current in ‘active’ pixel area which can lead to ‘latchup’.
- Processing just like CCD thinning for same silicon types
Back Illuminated CMOS Imagers

JAZZ II Backside CMOS minimal

Fe56 Kalpha
Fe55 Kbeta
Read noise < 2 e-
Si escape peak
Cr

Signal, e-
Teledyne HyViSI Devices – Hybrid Visible Silicon Imagers

Teledyne has developed a hybrid CMOS imager process much like IR detectors. Optimized silicon readout (ROIC) and optimized detector (silicon) allows high efficiency and low noise. Process has been aimed at high speed, but ultra low noise operation also possible.

- Formats up to 2kx2k, 18 um pixels
- < 10 electrons read noise
- 100% fill factor
Color Sensing – CMOS and CCD

Color filters placed over each pixel and imaging processing used to determine an ‘average color’ for each pixel based on local adjacent intensities.

Bayer pattern commonly used

low sensitivity and low spatial resolution compared to monochrome imagers due to filters